18ECPE705	VLSI TESTING	L	T	P	C
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Course Objectives:

1.	To gain the Basic knowledge on fault modelling, testing and test generation in logic circuit and delay test.
2.	To get exposure on testability approaches and test vector generation algorithms for logic circuits
3.	To understand the various fault diagnosis methods in logic systems

Unit I	TESTING AND TESTABLE DESIGN OF DIGITAL SYSTEMS	9	+	0

Need for testing - Fault models - Fault detection and redundancy - Combinational circuits – Sequential circuits - Fault equivalence - Fault dominance – Logic simulation - Compiler driven Simulation - Event driven Simulation - Fault simulation techniques - Serial, parallel, deductive.

Unit II	TESTING FOR SINGLE STUCK AT - FAULTS	9	+	0

Test generation algorithms for combinational circuits - Fault oriented ATG – D algorithm – Examples – PODEM – Fault independent ATG - Random test generation – ATG for SSFs in sequential circuits.

Unit III	DELAY TEST	9	+	0

Delay test problem – Path delay test – Transition faults – Delay test methodologies.

Unit IV	SELF-TEST AND TEST ALGORITHMS	9	+	0

Built-In Self Test - Test pattern generation for BIST - Circular BIST - BIST Architectures - Testable Memory Design - Test algorithms - Test generation for Embedded RAMs. FAULT DIAGNOSIS

Unit V	FAULT DIAGNOSIS	9	+	0

Logic Level Diagnosis - Diagnosis by UUT reduction - Fault Diagnosis for Combinational Circuits – Self checking design - System Level Diagnosis.

Total (L+T)= 45 Periods

Course Outcomes:

Upon completion of this course, the students will be able to:

CO1	:	Have basic knowledge on fault modelling, testing and test generation in logic circuits.
CO2	:	Understand the delay test methodologies.
CO3	:	Exposure to testability approaches and test vector generation algorithms for memory and logic Circuits
CO4	:	Understanding of the various fault diagnosis methods in logic systems.

Text Books:

1.	Abramovici M., Brever A., and Friedman D., "Digital Systems Testing and Testable Design", Jaico Publishing House, 2013.
2.	Michael L Bushnell and Vishwani D Agarwal, “Essentials of Electronic Testing for Digital, Memory and Mixed Signal Circuits”, Springer, 2002.

Reference Books:

1.	Stanley L Hurst “VLSI Testing : Digital and Mixed Analogue Digital Techniques”, Institute of Electrical Engineers,1998.
2.	Xiaoqing Wen, Cheng Wen Wu and LaungTerng Wang “VLSI Test Principles and Architectures: Design for Testability”, Morgan Kaufmann, 2011.
3	Parag K Lala, “Fault Tolerant and Fault Testable Hardware Design” BS Publications, 2002.
4.	A.L. Crouch, "Design Test for Digital IC's and Embedded Core Systems", Beijing China Electric Power Press, 2010.

E-References:

1.	https://nptel.ac.in/courses/106103116/handout/mod7.pdf
2.	http://www.ee.ncu.edu.tw/~jfli/soctest/lecture/ch03.pdf
3.	file:///C:/Users/admin/Downloads/chap1_lect00_testintro.pdf