22ECPE615	VLSI PHYSICAL DESIGN	SEMESTER VI

PRE-REQUISITE:	CATEGORY	PE	Credit		3
1. VLSI design 1. VLSI design	Hours/Week	L	T	P	TH
		3	0	0	3

Course Objectives:

1.	Understand the concepts of Physical Design Process such as partitioning, Floor planning, Placement and Routing.
2.	Discuss the concepts of design optimization algorithms and their application to physical design automation.
3.	Understand the concepts of simulation and synthesis in VLSI Design Automation Formulate CAD design problems using algorithmic methods.

Unit I	INTRODUCTION TO VLSI DESIGN AUTOMATION TOOLS	9	0	0	9

VLSI design automation tools- algorithms and system design. Structural and logic design. Transistor level design. Layout design. Verification methods. Design management tools.

Unit II	LAYOUT COMPACTION, PLACEMENT AND PARTITIONING	9	0	0	9

Layout compaction, placement and routing. Design rules, symbolic layout. Applications of compaction. Formulation methods. Algorithms for constrained graph compaction. Circuit representation. Wire length estimation. Placement algorithms. Partitioning algorithms.

Unit III	FLOOR PLANNING AND ROUTING	9	0	0	9

Floor planning and routing- floor planning concepts. Shape functions and floor planning sizing. Local routing. Area routing. Channel routing, global routing and its algorithms.

Unit IV	SIMULATION AND LOGIC SYNTHESIS AND VERIFICATION	9	0	0	9

Simulation and logic synthesis- gate level and switch level modeling and simulation. Introduction to combinational logic synthesis. ROBDD principles, implementation, construction and manipulation. Two level logic synthesis.

Unit V	HIGH-LEVEL SYNTHESIS	9	0	0	9

High-level synthesis- hardware model for high level synthesis. Internal representation of input algorithms. Allocation, assignment and scheduling. Scheduling algorithms. Aspects of assignment. High level transformations.

Total (45L)= 45 Periods

Text Books:

1.	S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley (India), 2006.
2.	N.A.Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer, 2012.

Reference Books:

1.	S.M. Sait, H. Youssef, "VLSI Physical Design Automation", Cambridge India, 2010.
2.	M.Sarrafzadeh, "Introduction to VLSI Physical Design", McGraw Hill (IE), 1996.
3.	Giovanni De Micheli, "Synthesis and Optimization of Digital Circuits", McGraw Hill, 2017
4.	Andrew B. Kahng and Jens Lienig "VLSI Physical Design: From Graph Partitioning to Timing Closure", Springer, 2011

E-References:

1.	https://nptel.ac.in/courses/106105161
2.	https://www.vlsi-expert.com/p/physical-design.html
3.	https://www.academia.edu/36687882/VLSI_Design_smd154_Physical_design_back_end

Course Outcomes: Upon completion of this course, the students will be able to:		Bloom's Taxonomy Mapped
CO1	Know to place the blocks and to partition the blocks while designing the layout for IC.	L2
CO2	Solve the performance issues in circuit layout.	L3
CO3	Analyze physical design problems and Employ appropriate automation algorithms for partitioning, floor planning, placement and routing	L4
CO4	Decompose large mapping problem into pieces, including logic optimization with partitioning, placement and routing	L3
CO5	Students are able to analyze circuits using both analytical and CAD tools.	L3

COURSE ARTICULATION MATRIX

COs/POs	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO1	PSO2	PSO3
CO1	1	1	1	1									1	1	
CO2	2	2	1	1									1		
CO3	2	2	1	1									1		
CO4	1	1	1	1		1							1	1	
CO5	3	3	1	1	3	1							1	2	3
Avg	1.8	1.8	1	1	0.6	0.4							1	0.8	0.6
3/2/1 - indicates strength of correlation (3-High,2- Medium,1- Low)															